WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

memory cells each of which includes a first MOS transistor with a stacked gate including a floating gate formed on a first well region formed at the surface of a semiconductor substrate with a gate insulating film interposed therebetween and a control gate formed on the floating gate with an inter-gate insulating film interposed therebetween, and a second MOS transistor having a drain connected to a source of the first MOS transistor;

a memory cell array which has the memory cells arranged in a matrix;

word lines each of which connects in common control gates of the first MOS transistors in a same row;

select gate lines each of which connects in common gates of the second MOS transistors in a same row;

a first row decoder which, in a write operation, selects any one of the word lines, applies a positive potential to the selected word line and applies a negative potential to the first well region, and after the write operation, brings the selected word line and the first well region into a floating state;

a second row decoder which selects any one of the select gate lines in a read operation; and

a control circuit which short-circuits the

selected word line and first well region in the floating state, the select gate lines being connected to a negative potential node in a write operation, and after the write operation, the select gate lines being isolated from the negative potential node and connected to the first well region.

2. The semiconductor memory device according to claim 1, wherein the first row decoder includes:

an address decode circuit which is provided for each of the word lines and which decodes a row address signal and, in a write operation, applies a positive potential to the selected word line;

a first switch element which connects a positive potential power supply node of the address decode circuit to a positive potential node;

a second switch element which connects the positive potential power supply node of the address decode circuit to the control circuit; and

a third switch element which connects a negative potential power supply node of the address decode circuit to a ground potential node, and

in the write operation, the first switch element connects the selected word line to the positive potential node via the positive potential power supply node of the corresponding address decode circuit and the third switch element connects the unselected word line to the ground potential node via the negative

potential power supply node of the corresponding address decode circuit, and

after the write operation, the first to third switch elements bring not only the positive potential power supply node and the negative potential power supply node of the address decode circuit into an open state to bring the selected word line into a floating state, and

after the selected word line is brought into the floating state, the second switch element connects the selected word line to the control circuit via the positive potential power supply node of the corresponding address decode circuit.

3. The semiconductor memory device according to claim 2, further comprising:

a fourth switch element which, in the write operation, connects the first row decoder to the control circuit to apply the negative potential supplied from the control circuit to the first well region via the first row decoder, after the write operation, disconnects the first row decoder from the control circuit to bring the first well region into the floating state and, after the first well region is brought into the floating state, connects the first row decoder to the control circuit to connect the control circuit and the first well region electrically; and

a fifth switch element which, when the fourth

switch element applies the negative potential to the first well region, connects the select gate line to the negative potential node and, when the first well region in the floating state is connected to the control circuit electrically, disconnects the select gate line from the negative potential node and connects the select gate line to the first well region.

4. The semiconductor memory device according to claim 3, wherein the first row decoder includes:

a third MOS transistor which is formed, for each of the select gate lines, on a second well region formed at the surface of the semiconductor substrate and isolated from the first well region, and which has one end of its current path connected to the fifth switch element and the other end of its current path connected to the select gate line; and

a sixth switch element which connects a negative potential power supply node of the address decode circuit to the control circuit, and

the third switch element further connects the negative potential power supply node of the address decode circuit to a negative potential node, and

in an erase operation, the third switch element connects the word line to the negative potential node via the negative potential power supply node of the corresponding address decode circuit, the fourth switch element connects the first row decoder to the control

circuit to apply a positive potential supplied from the control circuit to the first well region via the first row decoder, and the third MOS transistor is turned off, and

after the erase operation, the first to fourth switch elements and the sixth switch element are turned off to bring the word lines and the first well region into the floating state, and the third MOS transistor is in a off state, and

after the word lines and the first well region are brought into the floating state, the sixth switch element connects the word lines to the control circuit via the negative potential power supply node of the corresponding address decode circuit and the fourth switch element connects the first well region to the control circuit, and the third MOS transistor is in the off state.

5. The semiconductor memory device according to claim 1, further comprising:

bit lines each of which connects in common drains of the first MOS transistors in a same column electrically; and

a source line which connects in common sources of the second MOS transistors.

6. The semiconductor memory device according to claim 5, wherein each of the memory cells further includes a fourth MOS transistor which has a source

connected to the drain of the first MOS transistor and a drain connected to the bit line.

7. A semiconductor memory device comprising:

memory cells each of which includes a first MOS transistor with a stacked gate including a floating gate formed on a well region formed at the surface of a semiconductor substrate with a gate insulating film interposed therebetween and a control gate formed on the floating gate with an inter-gate insulating film interposed therebetween, and a second MOS transistor having a drain connected to a source of the first MOS transistor;

a memory cell array which has the memory cells arranged in a matrix;

word lines each of which connects in common the control gates of the first MOS transistors in a same row;

select gate lines each of which connects in common the gates of the second MOS transistors in a same row;

a first row decoder which, in a write operation, selects any one of the word lines, applies a positive potential to the selected word line and applies a negative potential to the well region, and after the write operation, brings the selected word line, the well region, and the select gate line into a floating state;

a second row decoder which selects any one of

the select gate lines in a read operation; and

a control circuit which short-circuits the word line, select gate line, and well region in the floating state.

8. The semiconductor memory device according to claim 7, wherein the first row decoder includes:

an address decode circuit which is provided for each of the word lines and which decodes a row address signal and, in a write operation, applies a positive potential to the selected word line;

a first switch element which connects a positive potential power supply node of the address decode circuit to a positive potential node;

a second switch element which connects the positive potential power supply node of the address decode circuit to the control circuit; and

a third switch element which connects a negative potential power supply node of the address decode circuit to a ground potential node, and

in the write operation, the first switch element connects the selected word line to the positive potential node via the positive potential power supply node of the corresponding address decode circuit and the third switch element connects the unselected word line to the ground potential node via the negative potential power supply node of the corresponding address decode circuit, and

after the write operation, the first to third switch elements bring the positive potential power supply node and the negative potential power supply node of the address decode circuit into an open state to bring the selected word line into a floating state, and

after the selected word line is brought into the floating state, the second switch element connects the selected word line to the control circuit via the positive potential power supply node of the corresponding address decode circuit.

9. The semiconductor memory device according to claim 8, further comprising:

a fourth switch element which, in the write operation, connects the first row decoder to the control circuit to apply the negative potential supplied from the control circuit to the well region via the first row decoder, after the write operation, disconnects the first row decoder from the control circuit to bring the well region into the floating state and, after the well region is brought into the floating state, connects the first row decoder to the control circuit to connect the control circuit and the well region electrically, wherein

the first row decoder further includes a third MOS transistor which is formed on the well region for each of the select gate lines, which has one end of its

current path connected to the well region and the other end of its current path connected to the select gate line, and which is turned on in the write operation.

10. The semiconductor memory device according to claim 9, wherein the first row decoder further includes a fifth switch element which connects the negative potential power supply node of the address decode circuit to the control circuit,

the third switch element further connects the negative potential power supply node of the address decode circuit to a negative potential node, and

in an erase operation, the third switch element connects the word line to the negative potential node via the negative potential power supply node of the corresponding address decode circuit, the fourth switch element connects the first row decoder to the control circuit to apply a positive potential supplied from the control circuit to the well region via the first row decoder, and the third MOS transistor is turned off, and

after the erase operation, the first to fifth switch elements are turned off to bring the word lines and the well region into the floating state and the third MOS transistor is in a off state, and

after the word lines and the well region are brought into the floating state, the fifth switch element connects the word lines to the control circuit

via the negative potential power supply node of the corresponding address decode circuit, the fourth switch element connects the well region to the control circuit, and the third MOS transistor is in the off state.

11. The semiconductor memory device according to claim 7, further comprising:

bit lines each of which connects in common drains of the first MOS transistors in a same column electrically; and

a source line which connects in common sources of the second MOS transistors.

12. The semiconductor memory device according to claim 11, wherein each of the memory cells further includes a fourth MOS transistor which has a source connected to the drain of the first MOS transistor and a drain connected to the bit line.

13. A semiconductor memory device comprising:

memory cells each of which includes a first MOS transistor with a stacked gate including a floating gate formed on a first well region formed at the surface of a semiconductor substrate with a gate insulating film interposed therebetween and a control gate formed on the floating gate with an inter-gate insulating film interposed therebetween, and a second MOS transistor which has a drain connected to a source of the first MOS transistor;

a memory cell array which has the memory cells arranged in a matrix;

word lines each of which connects in common the control gates of the first MOS transistors in a same row;

select gate lines each of which connects in common the gates of the second MOS transistors in a same row;

a first row decoder which, in an erase operation, applies a negative potential to the word lines, applies a positive potential to the first well region, and brings the select gate lines into a floating state, and after the erase operation, brings the word lines, the first well region, and the select gage lines into a floating state;

a second row decoder which selects any one of the select gate lines in a read operation; and

a control circuit which short-circuits the word lines and first well region in the floating state.

14. The semiconductor memory device according to claim 13, wherein the first row decoder includes:

an address decode circuit which is provided for each of the word lines and which decodes a row address signal and, in an erase operation, applies a negative potential to the word lines;

a first switch element which connects a positive potential power supply node of the address decode circuit to a positive potential node;

a second switch element which connects the negative potential power supply node of the address decode circuit to a negative potential node; and

a third switch element which connects the negative potential power supply node of the address decode circuit to the control circuit,

in an erase operation, the second switch element connects the word line to the negative potential node via the negative potential power supply node of the corresponding address decode circuit,

after the erase operation, the first to third switch elements bring the positive potential power supply node and negative potential power supply node of the address decode circuit into an open state to bring the word lines into a floating state, and

after the word lines are brought into the floating state, the third switch element connects the word line to the control circuit via the negative potential power supply node of the corresponding address decode circuit.

15. The semiconductor memory device according to claim 14, further comprising:

a fourth switch element which, in an erase operation, connects the first row decoder to the control circuit to apply the positive potential supplied from the control circuit to the first well region via the first row decoder, after the erase

operation, disconnects the first row decoder from the control circuit to bring the first well region into the floating state and, after the first well region is brought into the floating state, connects the first row decoder to the control circuit to connect the control circuit and the first well region electrically.

16. The semiconductor memory device according to claim 15, wherein the first row decoder further includes:

a third MOS transistor which is formed, for each of the select gate lines, on a second well region formed at the surface of the semiconductor substrate and isolated from the first well region and which has one end of its current path connected to the select gate line; and

a fifth switch element which connects the positive potential power supply node of the address decode circuit to the control circuit,

the device further includes a sixth switch element which switches the connection of the other end of the current path of the third MOS transistor to either the first well region or the negative potential node,

the second switch element further switches the connection between the negative potential power supply node of the address decode circuit and a ground potential node, and

in a write operation, the first switch element

connects the selected word line to the positive potential node via the positive potential power supply node of the corresponding address decode circuit, the second switch element connects the unselected word line, to the ground potential node via the negative potential power supply node of the corresponding address decode circuit, the fourth switch element connects the first row decoder to the control circuit to apply a negative potential supplied from the control circuit to the first well region via the first row decoder, the third MOS transistor is turned on, and the sixth switch element connects the other end of the current path of the third MOS transistor to the negative potential power supply node,

after the write operation, the first to fifth switch elements are turned off to bring the selected word line and the first well region into the floating state, and

after the selected word line and the first well region are brought into the floating state, the fifth switch element connects the selected word line to the control circuit via the positive potential power supply node of the corresponding address decode circuit, the fourth switch element connects the first row decode circuit to the control circuit to connect the control circuit and the first well electrically, and the sixth switch element connects the select gate line to the

first well region.

17. The semiconductor memory device according to claim 15, wherein the first row decoder further includes:

a third MOS transistor which is formed on the first well region for each of the select gate lines and which has one end of its current path connected to the select gate line; and

a fifth switch element which connects a positive potential power supply node of the address decode circuit to the control circuit,

the second switch element further switches the connection between the negative potential power supply node of the address decode circuit and a ground potential node, and

in an erase operation, the first switch element connects the selected word line to the positive potential node via the positive potential power supply node of the corresponding address decode circuit, the second switch element connects the unselected word lines to the ground potential node via the negative potential power supply node of the corresponding address decode circuit, the fourth switch element connects the first row decoder to the control circuit to apply a negative potential supplied from the control circuit to the first well region via the first row decoder, and the third MOS transistor is turned on,

after the write operation, the first to fifth switch elements are turned off to bring the selected word line, the first well region, and the select gate line into the floating state, and

after the selected word line is brought into the floating state, the fifth switch element connects the selected word line to the control circuit via the positive potential power supply node of the corresponding address decode circuit and the fourth switch element connects the first row decoder to the control circuit to connect the control circuit and the first well region electrically.

18. The semiconductor memory device according to claim 13, further comprising:

bit lines each which connects in common drains of the first MOS transistors in a same column electrically; and

a source line which connects in common sources of the second MOS transistors.

19. The semiconductor memory device according to claim 18, wherein the memory cell further includes a fourth MOS transistor having a source connected to the drain of the first MOS transistor and a drain connected to the bit line.